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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,064	09/23/2003	Been-Yih Jin	42P15997	2743

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,064	JIN ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *25-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,9-11,15,17-19 and 22* is/are rejected.

7)☒ Claim(s) *4,7,8,12-14,16, 20,21,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

6/15/05

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 050305
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

Remarks

1. The indication of allowable subject matter, as set forth in the previous Office action, is withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 6, 9-11, 15, 17-19 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by DE 19928564.

In re claim 1, DE19928564 teaches the claimed method comprising:

- forming a via layer 101/103 comprising a dielectric material (i.e. an oxide layer 101) on a semiconductor device substrate 100 (Fig.6 and col. 6, line 17);
- forming a trench layer 104-107 on the via layer 101 (Fig.6);
- forming a trench 107A and 107B through the trench layer 103-107 to expose the via layer 101/103 (Fig.7);
- forming a via 108 in the via layer 101/103 in the trench 107B to expose the substrate 100 (Fig.8); and
- forming a semiconductor material 102B (i.e. a polycrystalline silicon, col. 8, lines 11-13) in the via 108 and in the trench 107B (Fig.9).

In re claims 2-3, DE19928564 teaches forming the via layer 101/103 comprising forming a primary dielectric layer 101 comprising a material (i.e. the oxide) having a first etch characteristic; and forming a secondary dielectric layer 103 comprising a material (i.e. SiN) having a second etch characteristic different from the first etch characteristic.

In re claim 5, DE19928564 teaches planarizing an exposed surface of the semiconductor material 102B in the trench 107B (col. 7, lines 1-5).

In re claim 6, DE19928564 teaches planarizing the semiconductor material 102B in the trench 107B to a thickness suitable as a device channel (Fig.9).

In re claim 9, DE19928564 teaches forming a primary dielectric layer 105 and 107 (Fig.6) comprising a material (i.e. SiN, col. 6, lines 34-36) having a different etch characteristic different than a portion of the via layer (i.e. an oxide layer); and forming a secondary dielectric layer 104 and 106 comprising a material (i.e. polysilicon, col. 6, lines 22-24) having a different etch characteristic different than the primary dielectric layer (i.e. SiN).

In re claim10, DE19928564 teaches forming the primary dielectric layer 105 and 107 to a thickness selected to be suitable as a circuit device base.

In re claim 11, DE19928564 teaches further removing the trench layer 105 and 107 after forming the semiconductor layer 102A and 102B in the trench 107A and 107B (from Fig. 9 to Fig.10).

In re claim 15, DE19928564 teaches the claimed method comprising:

- forming a first dielectric layer 103 on a device substrate 100;

- forming a second dielectric layer 104 on the first dielectric layer 103, the second dielectric layer 104 comprising a material(i.e. polysilicon) having a different etch characteristic different than a material (i.e. SiN) of the first dielectric layer 103;
- forming a third dielectric layer 105 on the second dielectric layer 104, the third dielectric layer 105 comprising a material (i.e. SiN) having a different etch characteristic different than a material (i.e. polysilicon) of the second dielectric layer 104;
- forming a fourth dielectric layer 106 on the third dielectric layer 105, the fourth dielectric layer 106 comprising a material (i.e. polysilicon) having a different etch characteristic different than a material (i.e. SiN) of the third dielectric layer 105;
- forming a trench 107A and 107B through the third dielectric layer 105 (Fig.7);
- forming a via 108 in the trench 107B to expose the substrate 100 (Fig.8); and
- forming a semiconductor material 102B (i.e. a polycrystalline silicon, col. 8, lines 11-13) in the via 108 and in the trench 107B (Fig.9).

In re claim 17, DE19928564 teaches planarizing an exposed surface of the semiconductor material 102B in the trench 107B (col. 7, lines 1-5).

In re claim 18, DE19928564 teaches planarizing the semiconductor material 102B in the trench 107B to a thickness suitable as a device channel (Fig.9).

In re claim 19, DE19928564 teaches removing the third dielectric layer 105 and the fourth dielectric layer 106 after forming the semiconductor layer 102A and 102B in the trench 107A and 107B (from Fig. 9 to Fig.10).

In re claim 22, DE19928564 teaches that the first dielectric layer 103 and the third dielectric layer 105 comprises similar material(i.e. SiN) and the second dielectric layer 104 and the fourth dielectric layer 106 comprises similar material (i.e. polysilicon).

Allowable Subject Matter

4. Claims 4, 7, 8, 12-14, 16, 20, 21, 23 And 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record, DE 19928564, teaches a related art, as stated previously. In contrast, DE 19928564 at least neither teaches nor suggests that that the substrate comprises a *first semiconductor* material and a *second semiconductor* material on a portion of the first semiconductor material, the second semiconductor material has a different lattice parameter than the first semiconductor material; isolating the semiconductor material formed in the trench form a portion of the semiconductor material formed in the via; forming a trench pad having dimensions different than the trench adjacent to the trench; crystallizing the semiconductor material in the trench.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

June 15, 2005

HSIEN-MING LEE
PRIMARY EXAMINER

6/15/05